CLAIMS

1. A NAND flash memory cell array, comprising: a substrate having an active area, a plurality of vertically stacked pairs of floating gates and control gates arranged in rows above the active area, with the control gates being positioned above the floating gates, select gates aligned with and positioned on both sides of each of the stacked gates, a bit line above each row, a bit line diffusion in the active area toward a first end of each row, a bit line contact interconnecting the bit line in each row and the bit line diffusion, and a source region in the active area at least partially overlapped by the select gate at a second end of each row.

2. The memory cell array of Claim 1 wherein stacked gates and the stacked gates are self-aligned relative to each other.

3. The memory cell array of Claim 1 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

4. The memory cell array of Claim 1 wherein the control gates and the select gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during program and erase operations.

5. The memory cell array of Claim 1 wherein erase paths extend from the floating gates, through the tunnel oxide to the channel regions, and high voltage is coupled to the floating gates both from the control gates and from the select gates.

6. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to

the floating gates, and high voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region.

7. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation.

8. The memory cell array of Claim 1 wherein the select gates in unselected cells are biased at a relatively high voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source diffusion.

9. The memory cell array of Claim 1 wherein the bit line for a row containing a selected cell to be programmed is held at 0 volts, a relatively low positive voltage is applied to a cell select gate for the selected cell, a relatively high positive voltage is applied to the source diffusion at the second end of the row in which the selected cell is located, a relatively high positive voltage is applied to the control gate in the selected cell, a relatively high positive voltage is applied to the select gates for unselected cells, and a relatively high positive voltage is applied to the control gates in the unselected cells.

10. The memory cell array of Claim 1 wherein an erase path is formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusions, the source diffusion and the P-well at 0 volts.

11. The memory cell array of Claim 1 wherein an erase path is formed by a relatively high negative voltage on the control gates, and relatively low negative voltage on the select gates, with the P-well at a positive voltage and the bit line and source diffusions floating.

12. The memory cell array of Claim 1 wherein a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate at relatively high positive voltage, and the control gate of the selected cell is biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

13. The memory cell array of Claim 1 including an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

14. In a process of fabricating a NAND flash memory cell array, the steps of: forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, forming a dielectric film on the first silicon layer, etching away a portion of the dielectric film and the first silicon layer to form a row of select gates with exposed side walls, forming a first dielectric layer on the side walls of the select gates, forming a second silicon layer on the first dielectric layer, forming a second dielectric layer on the second silicon layer, forming a third silicon layer on the second dielectric layer, etching away portions of the third silicon layer to form control gates, etching away portions of the second silicon layer and the second dielectric layer to form floating gates which are thereby self-aligned with the control gates, forming bit line and source diffusions in the active area of the substrate between the select gates, and forming a bit line above the row and a bit line contact which interconnects the bit line and the bit line diffusion.

15. A NAND flash memory cell array, comprising: a substrate having an active area, a plurality of vertically stacked pairs of floating gates and control gates arranged in rows above the active area, with the control gates being positioned above the floating gates, select gates aligned with and positioned on both sides of each of the stacked gates, a bit line diffusion in the active area toward a first end of each row, a source diffusion in the active area directly beneath the select gate at a second end of each row, a bit line above each row, a bit line contact interconnecting the bit line in each row and the bit line diffusion.

16. The memory cell array of Claim 15 wherein the select gates are self-aligned to the stacked control and floating gates.

17. The memory cell array of Claim 15 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

18. The memory cell array of Claim 15 wherein the control gates and the select gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during program and erase operations.

19. A NAND flash memory cell array, comprising: a substrate having an active area, a plurality of vertically stacked pairs of floating gates and control gates arranged in rows above the active area, with the control gates being positioned above the floating gates, select gates aligned with and positioned on both sides of each of the stacked gates, a bit line above each row, a bit line diffusion in the active area toward a first end of each row, a bit line contact interconnecting the bit line in each row and the bit line diffusion, and a source region in the active area which is only partially overlapped by the select gate at a second end of each row.

20. The memory cell array of Claim 19 wherein the each of the floating gates and the control gate above it are self-aligned with respect to each other.

21. The memory cell array of Claim 19 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select gates, and a second relatively thick dielectric between floating gates and control gates.

22. The memory cell array of Claim 19 wherein the control gates and the select gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during program and erase operations.

23. A process of fabricating a NAND flash memory cell array, comprising the steps of: forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, etching away portions of the first silicon layer to form a strip of silicon which extends above the active area and in the direction of the row, forming a first dielectric film on the first silicon layer, forming a second silicon layer on the first dielectric film, forming a second dielectric film on the second silicon layer, etching away portions of the second silicon layer and the second dielectric film to form a row of control gates with exposed side walls, etching away portions of the first silicon layer and the first dielectric film to form floating gates which are stacked beneath and self-aligned with control gates, forming a source diffusion in the active area of the substrate next to the stacked gates at one end of the row, forming a third dielectric film on the side walls of the control and floating gates, depositing a third silicon layer over the third dielectric film, removing portions of the third silicon layer to form select gates on both sides of each of the stacked gates, with the select gate at the one end of the row being positioned directly above the source diffusion, forming a bit line diffusion in the active

area of the substrate near the select gate at the other end of the row, and forming a bit line above the row and a bit line contact which interconnects the bit line and the bit line diffusion.